Li Guangyan Gavin

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Product-driven PhD seeking full-time roles, **HK Permanent Resident**.

EDUCATION

Ph.D. Candidate, Electrical Engineering, City University of Hong Kong — 2020 — Feb 2025
Topic: Parallel computing, High-performance Computing with FPGA
Cumulative GPA: 3.82/4.3

BEng. 1st Class Hons., Electrical Engineering, City University of Hong Kong — 2016 — 2020

TOOLS AND SKILLS

Programming Languages: C/C++, Python(Numpy, Pandas), CUDA, Scala, Bash, Matlab.

C/C++ Development: CLion, Linux, Profilers(PyPerf, Perf, VTune), Git, CMake, CI/CD flow.

Hardware Development Tools: Xilinx Vivado, Xilinx Vivado HLS, Verilator, VCS.

Hardware Description Languages: Verilog, VHDL, System Verilog, Scala(Chisel, SpinalHDL).

Languages: Mandarin(Native), English(Proficient), Cantonese(Intermediate).

PROFESSIONAL EXPERIENCES

Huawei 2012 Laboratory, Theory Laboratory — Hong Kong
Research Intern — Dec 2023 — June 2024
- Contributed to a large-scale **optimization solver** project utilizing Intel x86 servers in an **HPC cluster**.
- Enhanced **SparseBLAS** operator in a **4×72-thread cluster** by 20% through optimized **memory allocation**.
- Cultivated a solid knowledge of industry-level **computing system** for low latency.

Zhejiang Lab — Hangzhou
Research Intern — July 2023 — Oct 2023
- Contributed to a **CUDA** library development project utilizing **NVIDIA A100 GPU**.
- Enhanced discrete convolution kernel through **kernel fusion**, improved over the open-source SoTA works.
- Contributed to migrate the NVIDIA GPU-based library to **Huawei NPU (ASCEND 910B)**.

SELECTED RESEARCH PROJECT

Design Space Exploration of Polynomial Multiplication Accelerator on FPGA — Hong Kong
- Proposed an innovative **low-latency** algorithm for discrete convolution.
- Designed a scalable accelerator, achieving a 35% performance improvement on Xilinx FPGAs.
- Cultivated a deep understanding of **parallel computing** and developed strong **project managing** skills.

Optimised Post-Quantum Cryptographic System on Embedded Linux — Hong Kong
- Proposed a low-complexity algorithm for discrete convolution reducing 10% mul operations.
- Developed a test suite with **PetaLinux** on the **ARM-FPGA platform** to facilitate functionality verification.
- Designing a embedded system enhanced by the proposed algorithm, achieving a 30% improvements.

Secure RISC-V Platform for IoT Devices — Hong Kong
- Developed a hardware accelerator for secure algorithms, interfacing with RISC-V processors via AXI DMA.
- Created a **C firmware** for booting and running a bare-metal IoT system.
- Collaborated with the team in task breakdown, brainstorming, and problem-solving activities.

SELECTED PUBLICATIONS

(**IF:7.7**) **Li, G.**, Chen, D., Mao, G., Dai, W., Sanka, A. I., and Cheung, R. C. (2023). Algorithm-Hardware Co-Design of Split-Radix Discrete Galois Transformation for KyberKEM. *IEEE Trans. Emerg. Top. Comput.*

(**IF:3.1**) **Li, G.**, Ye, Z., Chen, D., Dai, W., Mao, G., Huang, K. , and Cheung, R. C. (2024). ProgramGalois: A Programmable Generator of Radix-4 Discrete Galois Transformation Architecture for Lattice-based Cryptography. *ACM T. Reconfigurable Technol. Syst.*

(**IF:10.6**) Mao, G., Liu, Y., Dai, W., **Li, G.**, Zhang, Z., Lam, A. H. F., and Cheung, R. C. (2024). REALISE-IoT: RISC-V-Based Efficient and Lightweight Public-Key System for IoT Applications. *IEEE Internet Things J.*

Jin, S., Gu, Z., **Li, G.**, Chen, D., Koç, C. K., Cheung, R. C., and Dai, W. (2024). Efficient Key-Switching for Word-Type FHE and GPU Acceleration. *Under Review*

Mao, G., Chen, D., **Li, G.**, Dai, W., Sanka, A. I., Koç, Ç. K., and Cheung, R. C. (2022). High-Performance and Configurable SW/HW Co-design of Post-Quantum Signature CRYSTALS-Dilithium. ACM Transactions on Reconfigurable Technology and Systems.

PATENTS

Cryptosystem With Utilizing Split-Radix Discrete Galois Transformation (inventor) - U.S. Patent 2024/0430075 A1 - A method and system for key encapsulation processor for high performance.

A Processor For A Cryptosystem (inventor) - U.S. Patent 12,093,198 B2 - A method and system for digital signature service including hardware accelerator modules and software processor.

SELECTED AWARDS

Dec 2023 - 2023 Guangdong Province Computer Society Outstanding paper award - Third Prize

June 2023/June 2024 - Research Tuition Scholarship (RTS) - Full Tuition Fee

July 2023 - 2023 IC Design Invitational Competition for College Students from Across-the-Taiwan-Straits, Hong Kong and Macau - First Prize

Academic Year 2022/23 - CityU EE Graduate Research Seminar Awards - First Prize